Velicharla
Gokul Kumar

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About

As an experienced Front-End Chip Design Engineer, I specialize in digital circuit design and development for FPGA designs targeting ASIC flow. I have designed and implemented efficient RTL solutions, focusing on building robust, scalable hardware architectures for cutting-edge wireless systems, including implementation of 5G NR PHY DSP algorithm IPs on Hardware that meet project goals.

Skills

- **HDL:** Verilog and SystemVerilog for Digital Designing.
- **Tools & Simulation:** Experienced with Quartus, QuestaSim, Vivado and MATLAB.
- **RTL Design:** Familiar with PPA design trade-offs related to throughput, latency, Area; power optimization concepts; skilled in code linting and quality checks.
- **Timing Closure & CDC:** Knowledge of Static Timing Analysis (STA), constraint development, Clock Domain Crossing (CDC) techniques, and synchronization strategies.
- **SoC Architecture:** Familiar with ARM-based SoC designs.
- **Protocols & Interfaces:** Experience in AXI4-Stream; knowledge of AXI4, APB.
- **SerDes:** Knowledge on Ethernet IP integration and validation.
- **Scripting & Automation:** Good with Scripting languages such as Python, Makefile, Shell; experienced with automation tools like Jenkins and Docker.
- **Debugging & Problem Solving:** Strong debugging skills and a collaborative team player.

Experience

5G Testbed R&D Lab, Indian Institute of Technology Hyderabad *Dec 2023 – Present*
SoC RTL Design Engineer Hyderabad, India

- Designed and owned the Noise Covariance block for ULPI-powered 32TR O-RAN Massive MIMO radio unit, targeting high performance, area and timing goals.
- Knowledge on integrating high-speed Ethernet I/O interface IP, handling multi-clock domain designs with debugging in simulation and on hardware; contributed to micro-architecture and development of an Ethernet debug architecture enabling a 25G SFP link for O-RAN mMIMO ULPI IP.
- Collaborated with cross-functional teams including architecture, validation and software teams to enable HW–SW co-design and integrated new features into the SoC.
- Delivered good RTL designs with comprehensive technical documentation, architecture reviews and structured hand-off documentation.
- Debugged and optimized modem core IPs for the 5G NR UE PHY Baseband subsystem, with a focus on the Synchronization Signal Block (SSB) Receiver chain.
- Identified areas for automation and create solutions to improve productivity, continuously improved the automation process by exploring new tools and technologies to execute test plans and analyzed the results.

5G Testbed R&D Lab, Indian Institute of Technology Hyderabad *Mar 2023 – Nov 2023*
Research Project Trainee Hyderabad, India

- Assisted in developing fundamental DSP modules with fixed-point implementation in HDL, focusing on synthesis, optimization and code linting.
- Integrated Soft interface IPs such as DDR4 controller from reference design and DMA to support required system functionality.
- Developed Make, Tcl, and Python scripts to automate EDA tool flows and performed unit testing with Cocotb for developer sanity checks.

Indian Institute of Technology Hyderabad *Aug 2022 – Feb 2023*
Future Wireless Communications Intern Hyderabad, India

- Designed and implemented basic DSP modules using High-Level Synthesis (HLS).
- Applied matrix analysis and optimization techniques (cvxpy, gradient ascent, and descent) in Python.
- Developed digital logics with PlatformIO, Arduino, and IDF frameworks in Verilog, Assembly, and Avr-gcc.

Education

Vignan's Foundation for Science Technology and Research — AP, India
B.Tech in Electronics and Communication Engineering; — *2019 – 2023*
CGPA: 9.52/10.0

Sri Chaitanya Jr. College — AP, India
MPC; — *2017 – 2019*
CGPA: 9.88/10.0

Sri Chaitanya Techno School — AP, India
SSC; — *2017*
GPA: 9.8/10.0

Key Projects

- **5G-NR ORAN ULPI.**
- **5G-NR mmWave UE CPE/Modem.**

Volunteer Experience

- **IEEE Student Branch Secretary:** 6 Months.
- **Class Representative:** 6 Months.
- **Student Coordinator:** 3 Days
  - CIRH International Conference.

Certifications

- VLSI Physical Design (NPTEL)
- Problem Solving Through Programming in C (NPTEL)
- Programming, Data Structures and Algorithms Using Python (NPTEL)
- Programming For Everybody (Coursera)
- Programming In Java (NPTEL)
- Business English Certificate Vantage (CEFR Level: B1)
- DevOps and Building Automation using Python (Coursera)

Awards & Activities

- **Merit Certificate:** Certificate of academic excellence (2020, 2021).
- **Sports:** Badminton.